Geunyeol Yu

Ph.D. Candidate

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Research Interests

My research focuses on developing secure and reliable systems using formal methods such as model checking, rewriting logic, and SMT solving. I am currently working on:

- Model checking of Signal Temporal Logic (STL) properties in cyber-physical systems
- Formal specification and analysis of Trusted Execution Environments (TEEs)
- Development of an extensible framework that integrates rewriting logic with SMT solving

Education

POSTECH (Pohang University of Science and Technology) Integrated M.S. & Ph.D. in Computer Science and Engineering	Mar 2019 – Present
Advisor : Prof. Kyungmin Bae POSTECH (Pohang University of Science and Technology) B.S. in Computer Science and Engineering	Mar 2012 – Feb 2019
Work Experience	
Software Engineer Intern	Hwasung, South Korea
Samsung Electronics DS AI Center	Feb 2023 – Mar 2023
$\circ~$ Developed GUI test suites for web services and conducted testing	
Software Engineer Intern	Seongnam, South Korea
Naver Webtoon	Jul 2018 – Aug 2018
$\circ~$ Refactored Android client by migrating the code base from Java to Kotlin	
Communications Specialist, Signal Corps (mandatory service)	Seoul, South Korea
ROK Defense Communication Command	Jan 2016 – Oct 2017
$\circ~$ Maintained and secured tactical communication networks	
QA Engineer Intern	Seongnam, South Korea
SK Hynix	Dec 2014 – Jan 2015

• Performed testing for NAND firmware

Publications

I have published papers at conferences, journals, and workshops related to formal methods, verification, and software engineering, such as CAV (2022), ASE (2021), FASE (2024), SCP (2025), and WRLA (2019, 2024).

[J1] SMT-Based Robust Model Checking for Signal Temporal Logic Jia Lee, Geunyeol Yu, Kyungmin Bae Science of Computer Programming, 2025 10.1016/j.scico.2025.103332 ☑

[C1] Formal Specification of Trusted Execution Environment APIs Geunyeol Yu, Seunghyun Chae, Kyungmin Bae, Sungkun Moon International Conference on Fundamental Approaches to Software Engineering (FASE), 2024 10.1007/978-3-031-57259-3_5 ☑

Geunveol Yu, Kyungmin Bae International Workshop on Rewriting Logic and its Applications (WRLA), 2024 10.1007/978-3-031-65941-6_10 **8** Best Paper/Presentation Award for Young Researcher [C2]STLmc: Robust STL Model Checking of Hybrid Systems Using SMT Geunyeol Yu, Jia Lee, Kyungmin Bae International Conference on Computer Aided Verification (CAV), 2022 10.1007/978-3-031-13185-1_26 [C3]Efficient SMT-based Model Checking for Signal Temporal Logic Jia Lee, Geunyeol Yu, Kyungmin Bae International Conference on Automated Software Engineering (ASE), 2021 10.1109/ASE51524.2021.9678719 [W2]Maude-SE: a Tight Integration of Maude and SMT solvers Geunveol Yu, Kyungmin Bae International Workshop on Rewriting Logic and its Applications (WRLA), 2020 Academic Activities Artifact evaluation committee member • International Conference on Computer Aided Verification (CAV), 2025 **Research Fundings Principal Investigator** Search and Deduction Technique for Efficient Model Checking of CPS Software Sep 2024 – Aug 2026 Supported by Basic Science Research Program, National Research Foundation of Korea funded by the Ministry of Education (Grant No. RS-2024-00413206) Honors and Awards • Research Subsidies for Ph.D. Candidates, National Research Foundation of Korea 2024• Best Paper/Presentation Award, WRLA 2024• POSTECH CSE Paper Award 2023 • National Science & Technology Scholarship 2012-2015, 2018 Software STLmc https://stlmc.github.io • An SMT-based model checker for robust verification of signal temporal logic properties in hybrid systems MaudeSE https://maude-se.github.io • An SMT extension of Maude (a high-performance reflective language and system supporting equational and *rewriting logic* specification and programming)

A Flexible Framework for Integrating Maude and SMT Solvers Using Python

Formal specification of TEE

- $\circ \ https://github.com/postechsv/tee-formal-spec$
- Maintainer & Main developer (2023 Present)

Teaching Experience

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[W1]

Theory of Computation (CSED502), Teaching Assistant, POSTECH	Fall 2024
Software Design Methods (CSED332), Teaching Assistant, POSTECH	Fall 2019, Fall 2020
Programming Languages (CSED321), Teaching Assistant, POSTECH	Spring 2019

Talks

- Formal Specification of Trusted Execution Environment APIs, Paper presentation at the Apr 2024
 [T1] 27th International Conference on Fundamental Approaches to Software Engineering (FASE'24), Luxembourg City, Luxembourg
- A Flexible Framework for Integrating Maude and SMT Solvers Using Python, Pa- Apr 2024
 [T2] per presentation at the 15th International Workshop on Rewriting Logic and its Applications (WRLA'24), Luxembourg City, Luxembourg
- [T3] Formal Specification of Trusted Execution Environment APIs, Invited talk, KAIST Feb 2024 PLRG Seminar, Daejeon, South Korea
- **[T4]** The STLmc tool demonstration, Tool demonstration at the 34th International Conference Aug 2022 on Computer Aided Verification (CAV'22), Haifa, Israel
- [T5] Maude-SE: A Tight Integration of Maude and SMT Solvers, Paper presentation at the Oct 2020 13th International Workshop on Rewriting Logic and its Applications (WRLA'20), online